

Processor Architecture

This unit covers advanced topics within processor architecture. It looks at structures of both uniprocessor systems and multiprocessor systems.

Overview: Processor Design: Advanced Topics · Survey of High Performance Architectures · CPU Organization Overview · Advanced Topics in Microarchitecture

Prerequisites: Computer Architecture

Topics	References	Tutorials	Patents
Pipelining (Stall, Bubble, Multiple, Flush) [+]		<ul style="list-style-type: none"> • Tutorial: Pipelining • Pipelining • Instruction Pipelining • Advanced Issues in Pipelining 	
Superscalar Architecture [+]	<ul style="list-style-type: none"> • Asynchronous Superscalar Architecture • Superscalar Processor Architecture 	<ul style="list-style-type: none"> • The Superscalar Hardware Architecture of the MC68060, Joseph Circello, Computer Museum History Center, Video (25 minutes), Hot Chips VI - 1994 [8/15/1994 1 PM (Pacific)] 	
VLIW [+]		<ul style="list-style-type: none"> • VLIW/Superscalar Processors 	
Multiprocessors [+]		<ul style="list-style-type: none"> • Multiprocessor Systems • Parallel Processors • Scalable Multiprocessors and the DASH Approach John Hennessy Video (52 minutes) Computer Museum History Center 4/10/1992 1 PM (Pacific) • Cache-Coherent Multiprocessors: an Easy Approach to High-Performance Computing Forest Baskett Video (40 minutes) Computer Museum History Center 10/18/1990 1 PM 	

Multithreaded Processors [+]

- Multithreading documents list
- M. J. Flynn and A. Podvin, *Shared Resource Multiprocessing*, IEEE Computer, pp. 20-28, March 1972.

(Pacific)

- 5430851

Trace Processing [+]

- Reference list
- Trace Processors
- Rotenberg, Eric, *Trace Processors: Exploiting Hierarchy and Speculation*, Doctorial Thesis, University of Wisconsin-Madison, 1999.
- Trace Processors and Control Independence

Eric Rotenberg, Video (60 minutes)
[4/20/1999 3:30 PM (Pacific)]

Reconfigurable Processors, FPGA [+]

- Reference list
- DRHW WWW Library
- Adaptive hardware becomes a reality using electrically reconfigurable arrays (ERAs)
- The Nano Processor: a low resource reconfigurable processor
- The implementation of hardware subroutines on field programmable gate arrays

• Reconfigurable Computing

Memory Hierarchy* [+]

- Memory Hierarchy in Cache Based Systems
- CPUs combined with bulk memory reference list
- Memory accessing (e.g. prefetch) and RAMBUS reference list

• Memory Hierarchy Overview

Vector Processors [+]

- Vector Processors Overview
- Vector pipelining, chaining, and speed on the IBM 3090 and Cray X-MP

• Vector Processing

SIMD [+]

- SIMD Instructions
- SIMD Architectures

BEST AVAILABLE COPY

MIMD [+]

- MIMD Architectures

Advanced Units: Instruction Sets · Memory Data Flow Techniques · Register Data Flow Techniques

* Denotes a topic that is useful but not necessary.

NORTH: North Online Relational Training Hierarchy

Developed by: Nick Galotti, Justin Marrese, Maulin Patel, Mike Pyzocha as part of a project for WPI

BEST AVAILABLE COPY

Computer Architecture

Computer Architecture is the study of the interconnection of the various components of a computer. The goal of this unit is to provide detailed information about the architecture of the many components of a computer.

Overview: WWW Computer Architecture ·

Book: Computer Architecture: A Quantitative Approach

Author: Hennessy and Patterson

ISBN: 1558605967

Prerequisites: Micro Processor Systems · VLSI Systems · Operating Systems

Topics

Computer Organization [+]

References

- Anatomy of Modern Processors

Tutorials

- Computer Organization
- Slides from technical training classes

Patents

- I/O Systems
- Memory Systems
- Pipelines

Processors and Systems [+]

I/O Systems [+]

Memory Systems [+]

Pipeline Structures [+]

Advanced Units: Processor Architecture · Instruction Processing

* Denotes a topic that is useful but not necessary.

NORTH: North Online Relational Training Hierarchy

Developed by: Nick Galotti, Justin Marrese, Maulin Patel, Mike Pyzocha as part of a project for WPI

BEST AVAILABLE COPY